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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,697	10/28/2003	George Keith Parish	2003-0213.02 (58532.US/46	3917

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EXAMINER	
VO, ANH T N	

ART UNIT	PAPER NUMBER
2861	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,697	PARISH ET AL.	
	Examiner	Art Unit	
	Anh T.N. Vo	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-19* is/are allowed.

6)☒ Claim(s) *1,8 and 9* is/are rejected.

7)☒ Claim(s) *2-7 and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The references cited on PTO 1449 have been considered

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 4, 6, 9 and 17 are objected to because of the following informalities:

- In claim 4, line 6, "the switches said control" should be corrected as --the switches, said control--.
- Claim 6 is objected to because it is a duplicate of claim 5.
- In claim 9, line 9, "one ink ejectors" should be corrected as --one ink ejector--.
- In claim 17, line, "signals, (A1 and A2)" should be corrected as --signals (A1 and A2)--.

Appropriate correction is required.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, the recitation "ink" on line 5, "data signals" on line 6 and "selected ejectors" on line 7 is confusing because it is unclear if this is additional "ink", "data signals" and "selected ejectors" or further recitation of the previously claimed "ink" on line 3, "data signals" on line 1 and "selected ink ejectors" on line 4. The same is true for reciting "a compensation circuit" on line 1 of claim 2, "a single compensation circuit" on lines 17-18, a single associated ink ejector" on line 19 and "ink" on line 21 of claim 8, and "a compensation circuit" on line 2 of claims 9-12. Also, the recitation "the resistance" and "the control signal" on line 9 lacks antecedent basis. It is unclear how the ejectors can be "selected" since no means for providing a "selecting function" is recited in claim and what the "parameter conditions" on line 11 are.

In claim 3, it is unclear what the "defined group" on line 9 is and how the group can be defined. The same is true for reciting "defined group" in claims 5 and 6-7.

In claim 5, the recitation "the number of ink ejectors" on line 2 lacks clear antecedent basis. The same is true for reciting "the number of ink ejectors" in claims 6-7.

In claim 8, it is unclear what the "logic" on line 12 is. The same is true for claims 13-14.

In claim 9, it is unclear what the "particular ink ejector" the "particular power signal" are. The same is true for claims 10-12.

In claim 10, it is unclear how the switches can be "selected" on line 1 since no means for providing the selecting function is recited in the claim.

In claim 13, it is unclear what the "object" and "address dimensions" on line 4, "unique combination" on line 12, "unique group of ejectors" on line 14 and "particular number of switches" on line 25 are and how the address can have dimensions. Also, the recitation "first dimension signals" and "a second dimension signals" on line 13 and "a single compensation circuit" on line 21 and 23 is confusing because it is unclear if these are additional "first dimension signals", "a second dimension signals" and "a single compensation circuit" or further recitation of the previously claimed "first dimension signals" and "a second dimension signals" on line 6 and "a single compensation circuit" on lines 21 and 23. The same is true for reciting "logic" on line 2 of claims 14-15.

In claim 14, i.e., the recitation "the number of switches" on line 2, "the particular power signal" on line 4, "the particular unique group of ejectors" on line 4 and "the predetermined time" on line 7 lacks clear antecedent basis. It is what the "particular compensation circuit" on

line 3, "the particular power signal" and "the particular unique group" are. The same is true for claims 15-16.

In claim 17, the recitation "A and B power signals", "two first dimension address signals", "two second dimension signals" on lines 2-3, and "ink ejectors" on lines 5-6 is confusing because it is unclear if this is additional address signals, dimension signals and ink ejectors or further recitation of the previously claimed "power signals" on line 3, "address dimensions" on line 5 and "ink ejectors" on line 14 of claim 13. Also, it is unclear what the "ejectors 1, 2, 3, 4" on line 29 and "switches 1&2, 3&4, 5&6 and7&8", "ejectors 1-4" on line 35 and "ejectors 5-8" on line 36 are and if they are additional "ejectors" and "switches" or further recitation of the previously claimed "ejectors" on line 28 and "switches" on line 29. The same is true for reciting "M groups of ink ejectors" on line 2 and logic gates" on line 4 of claim 18.

In claim 18, the recitation "the address signals" on line 5 lacks clear antecedent basis. It is unclear where these signals come from.

In claim 19, the recitation "the number" on line 2 lacks clear antecedent basis.
The remaining claims are dependent from the above claims and therefore also considered indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 8-9 are rejected under 35 USC 102 (b) as being anticipated by Misumi (US 6,431,685).

Misumi discloses in Figures 5-10 a printer comprising:

- a printer electronics (23-25), a media carrier (not shown), control signals from a latch (3)

and data signals from a latch (33)
- a printhead (21) mounted on the carrier (100); the printhead including:
- a plurality of ink ejectors (1) for ejecting ink when actuated;
- a power circuit (not shown) for selectively applying power (11) to selected ink ejectors (1) to actuate the ink ejectors and eject ink;
- a control circuit (3,14, 33) having logic gates (14) responsive to data signals from the latches (3, 33) for controlling the operation of the power circuit to actuate selected ejectors (1) based on the data signals; and
- wherein the power circuit including a compensation circuit (2, 30A-30C) controlled by the control circuit for reducing the resistance of the power circuit in response to the control signals, see lines 9-50, column 6. The resistance of the compensation circuit is reduced when the transistors associated with the resistor 30A is selected in response to predetermined parameter conditions to increase the conducting current to 75.5mA since the resistor (30A) has a lower resistance.

With regard to claim 9, wherein the logic (14) is configured to actuate only one switch of the X number of switches (3) in the compensation circuit to actuate a particular ink ejector when the following conditions exist: (1) the particular ink ejector is associated with a particular power signal (11) and only one of the ink ejectors associated with the particular power signal (11) be actuated in a predetermined time interval based on the data signals from latches (3) (column 6, lines 10-35).

Allowable Subject Matter

Claims 2-7 and 10-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The claims are allowable because the prior art of record does not show:

- The control circuit being interconnected with said first and second switches for switching the first and second switches on, whereby the resistance of the compensation circuit may be

reduced by switching both the first and second switches on as compared to switching on only the first switch as combined in claims 2-3.

- The control circuit actuate a select number of X number of switches based on upon the data signals as combined in claims 4-7, 10-12 and 14-16.
- A plurality of ink ejectors disposed in the printhead for ejecting ink, each ink ejector being uniquely identified with a unique combination of the power signals, first dimension signals and a second dimension signals and each power signal being associated with and providing power to a unique group of ejectors as combined in claim 13.
- The control circuit comprises first AND to seventh AND gate and ink ejectors 1-4 are in a first group connected to A power line and ink ejectors 5-8 are in a second group connected to the B power line as combined in claim 18.
- The control circuit comprises a counter and the logic gates is responsive to the counts to actuate a particular number of switches as combined in claim 19.

Citation of Pertinent Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art references (US Pat. 5,163,760; US Pat. 5,526,027; US Pat. 5,767,872; US Pat. 5,786,837; US Pat. 6,439,678; US Pat. 6,755,495) cited in the PTO 892 form show a thermal ink jet printer that is deemed to be relevant to the present invention. These references should be reviewed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Anh Vo whose telephone number is (571) 272-2262. The examiner can normally be reached on Tuesday to Friday from 8:30 A.M.to 6:30 P.M..

The fax number of this Group 2861 is (703) 872-9306.

ANH T.N. VO
PRIMARY EXAMINER
April 13, 2005